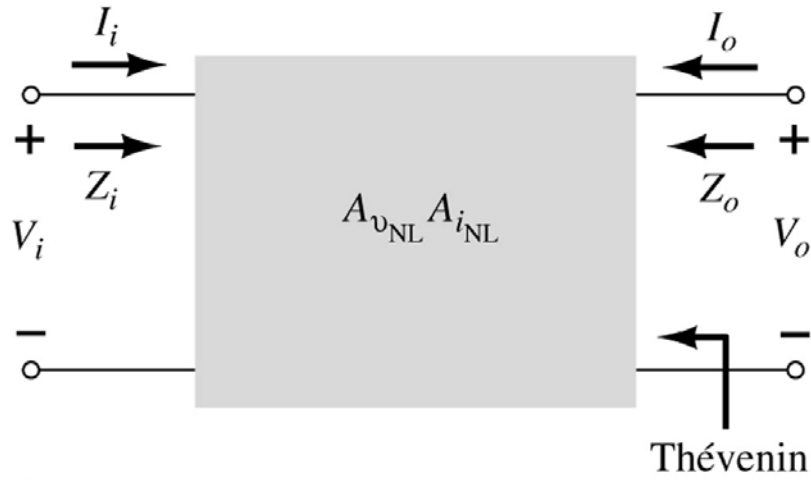


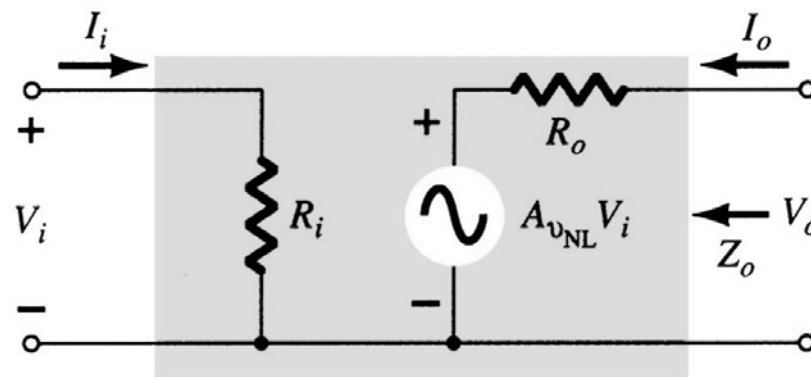
FIGURE 10-1 Two-port system.



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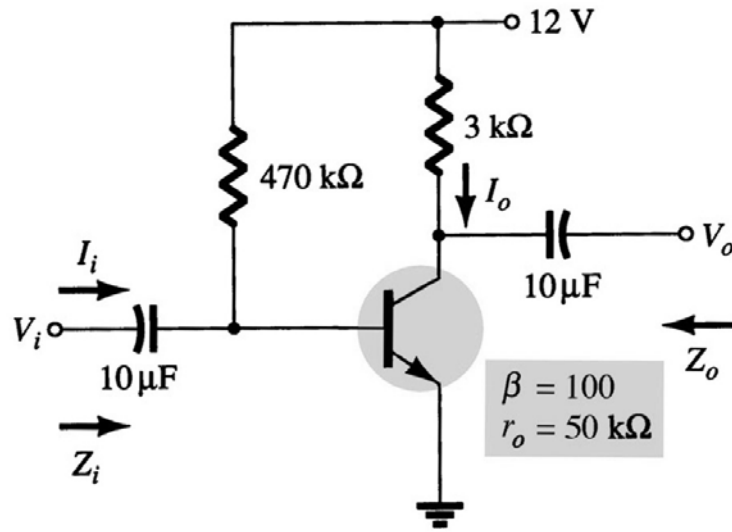
FIGURE 10-2 Substituting the internal elements for the two-port system of Fig. 10-1.



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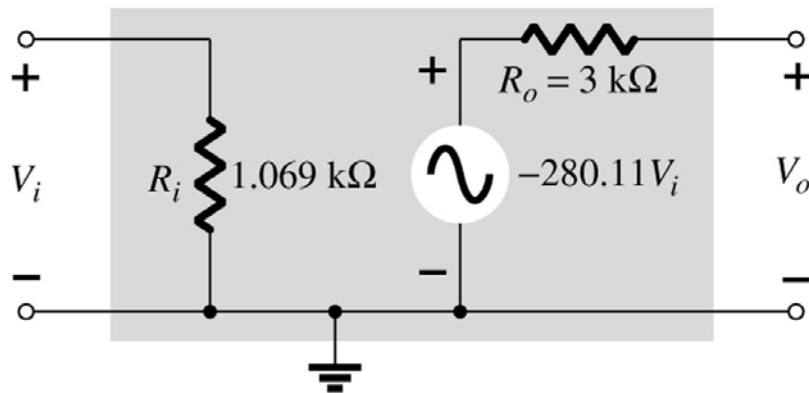
FIGURE 10-3 Example 10.1.



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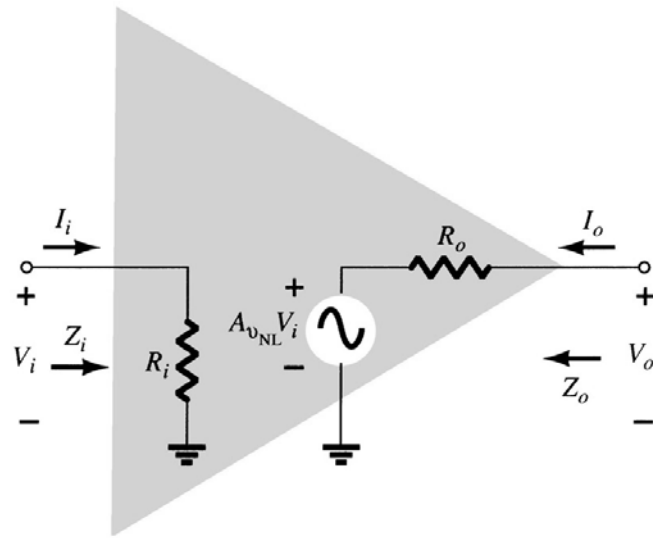
FIGURE 10-4 Two-port equivalent for the parameters specified in Example 10.1.



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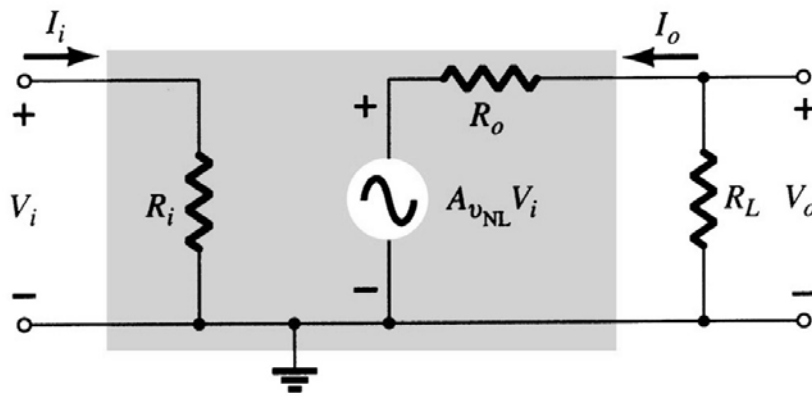
FIGURE 10-5 Operational amplifier (op-amp) notation.



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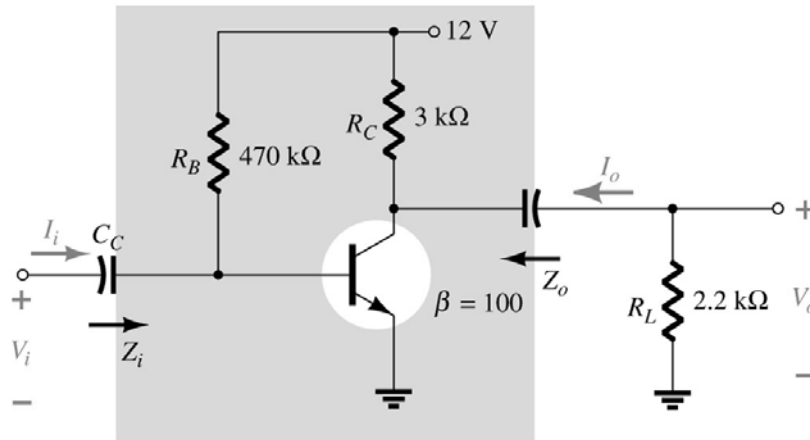
FIGURE 10-6 Applying a load to the two-port system of Fig. 10-2.



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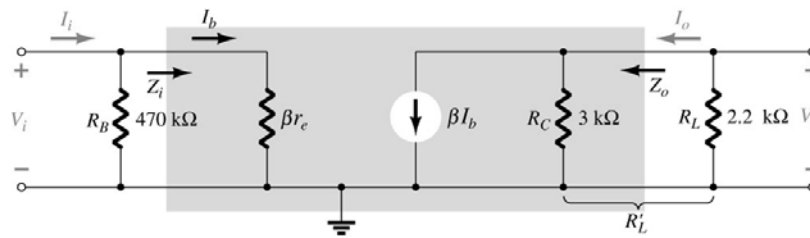
FIGURE 10-7 Example 10.2.



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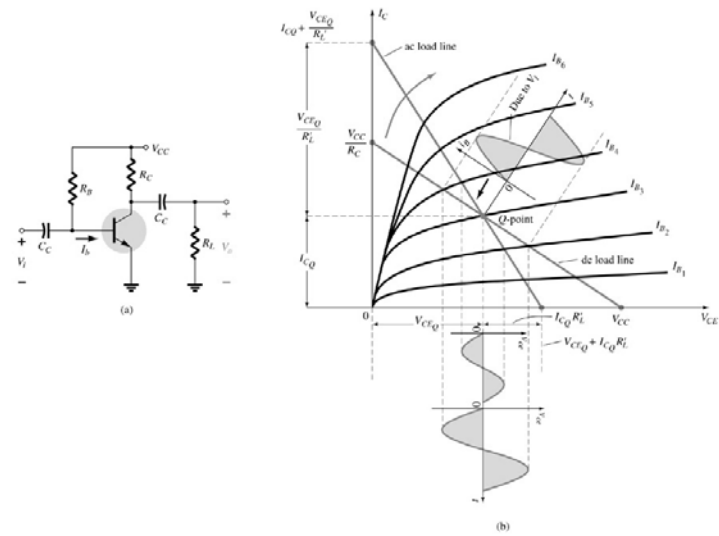
FIGURE 10-8 Substituting the r_e model in the ac equivalent network of Fig. 10.7.



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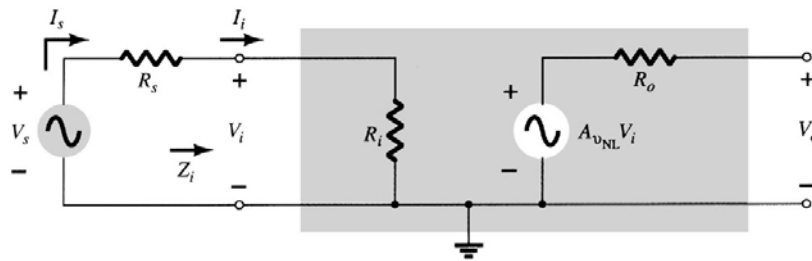
FIGURE 10-9 Demonstrating the differences between the dc and ac load lines.



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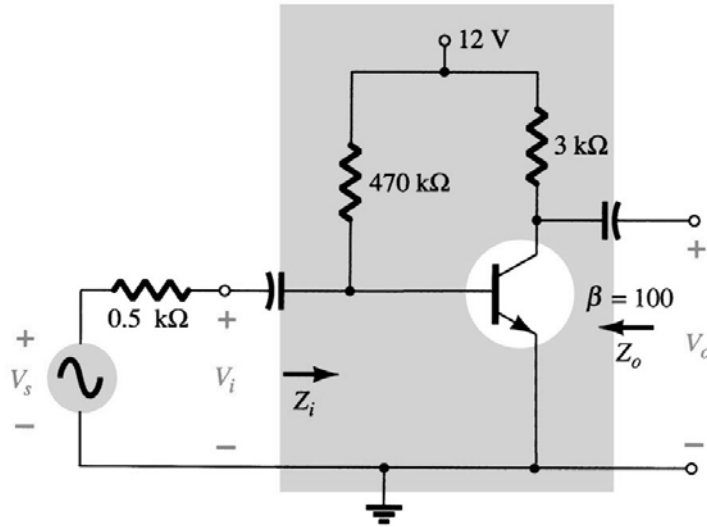
FIGURE 10-10 Including the effects of the source resistance R_s .



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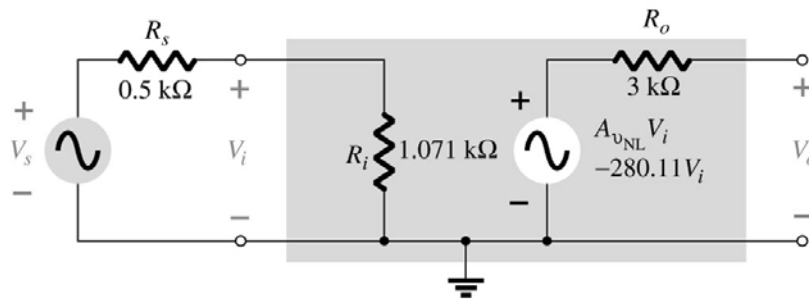
FIGURE 10-11 Example 10.3.



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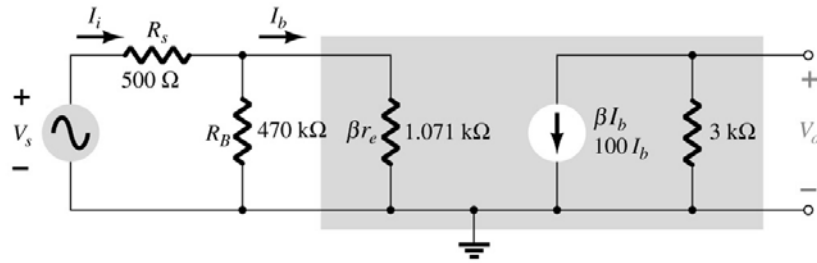
FIGURE 10-12 Substituting the two-port equivalent network for the fixed-bias transistor amplifier of Fig. 10-11.



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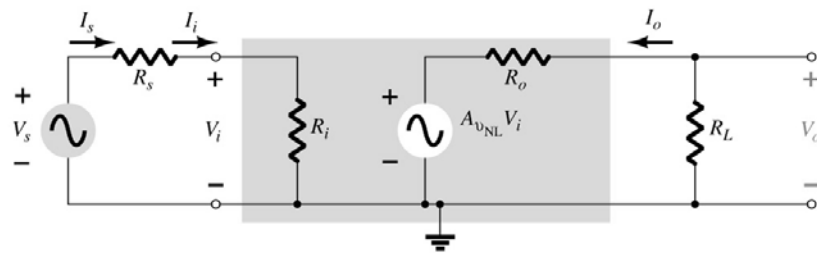
FIGURE 10-13 Substituting the r_e equivalent circuit for the fixed-bias transistor amplifier of Fig. 10-11.



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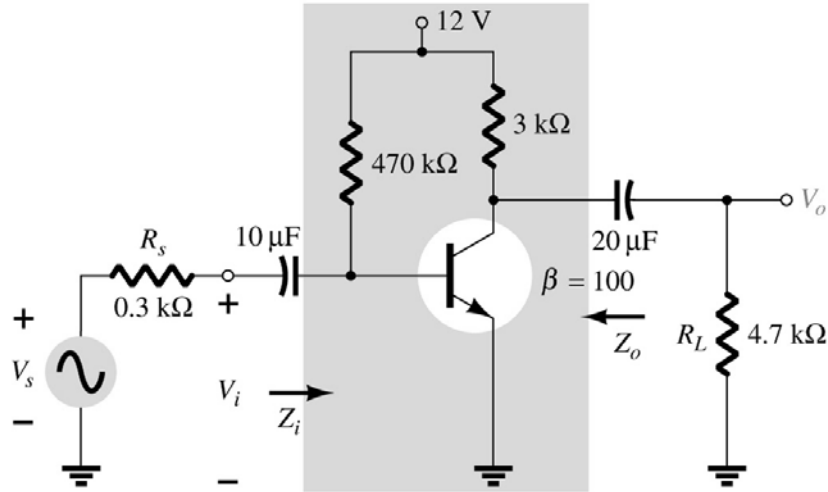
FIGURE 10-14 Considering the effects of R_s and R_L on the gain of an amplifier.



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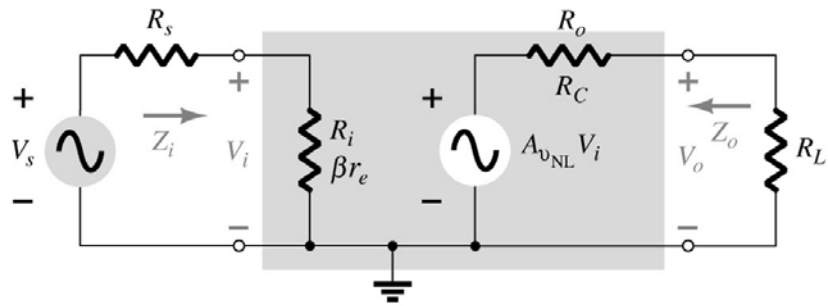
FIGURE 10-15 Example 10.4



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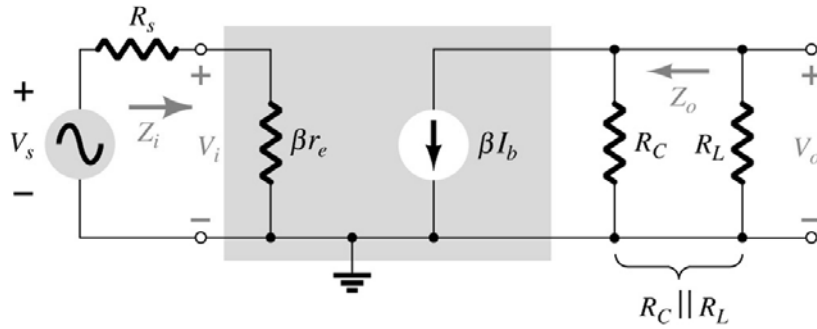
FIGURE 10-16 Fixed-bias configuration with R_i and R_o .



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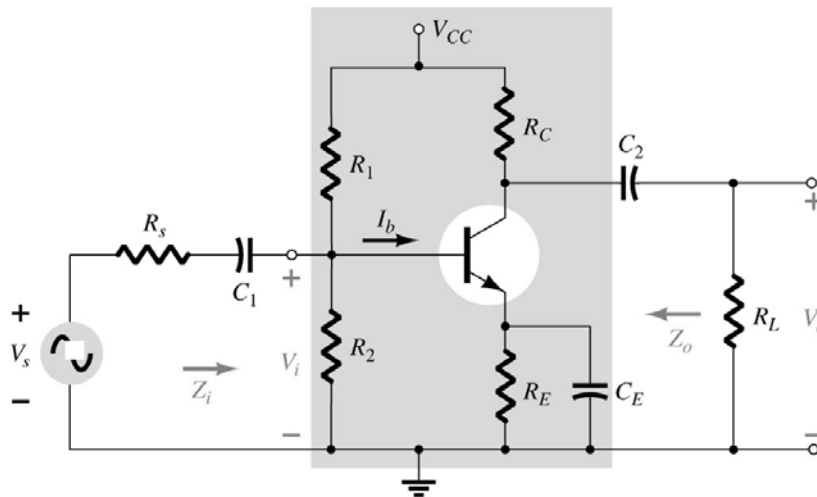
FIGURE 10-17 Fixed-bias configuration with the substitution of the r_e model.



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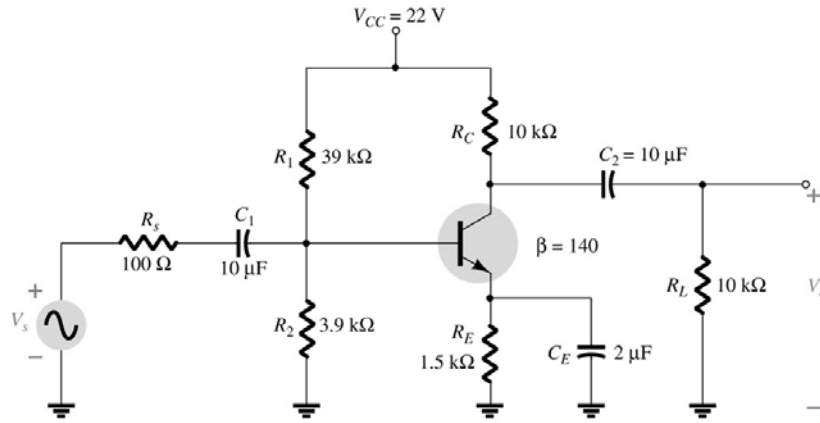
FIGURE 10-18 Voltage-divider bias configuration with R_1 and R_2 .



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FIGURE 10-19 Loaded voltage-divider BJT configuration to be analyzed using Mathcad.



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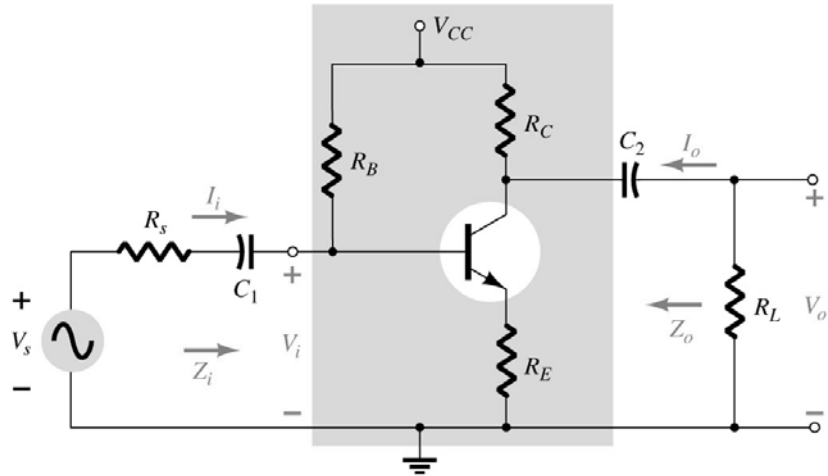
FIGURE 10-20 Mathcad analysis of Fig. 10-19.

$R1 := 39 \cdot 10^3$	$R2 := 3.9 \cdot 10^3$	$RC := 10 \cdot 10^3$	$RE := 1.5 \cdot 10^3$	
$VCC := 22$	$\beta := 140$	$VBE := 0.7$	$RL := 10 \cdot 10^3$	$RS := 100$
$RTh := \frac{R1 \cdot R2}{R1 + R2}$	$ETh := \frac{R2 \cdot (VCC)}{R1 + R2}$			
$IB := \frac{ETh - (VBE)}{RTh + (\beta + 1) \cdot RE}$	$IB = 6.045 \cdot 10^{-6}$			
$IE := (\beta + 1) \cdot IB$	$IE = 8.524 \cdot 10^{-4}$			
$re := \frac{26 \cdot (10^{-3})}{IE}$	$re = 30.503$			
$Zi := RTh \cdot \beta + \frac{re}{\beta + 1}$	$Zi = 1.937 \cdot 10^3$			
$Zo := RC$	$Zo = 1 \cdot 10^4$			
$Av := -\frac{RC \cdot (RL)}{re \cdot (RC + RL)}$	$Av = -163.919$			
$Avs := \left[\frac{Zi}{Zi + RS} \right] \cdot Av$	$Avs = -155.872$			

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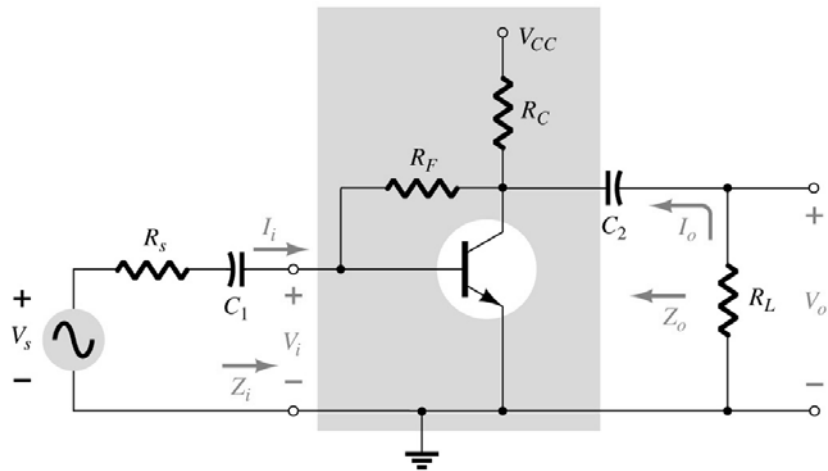
FIGURE 10-21 CE unbypassed emitter-bias configuration with R_s and R_L .



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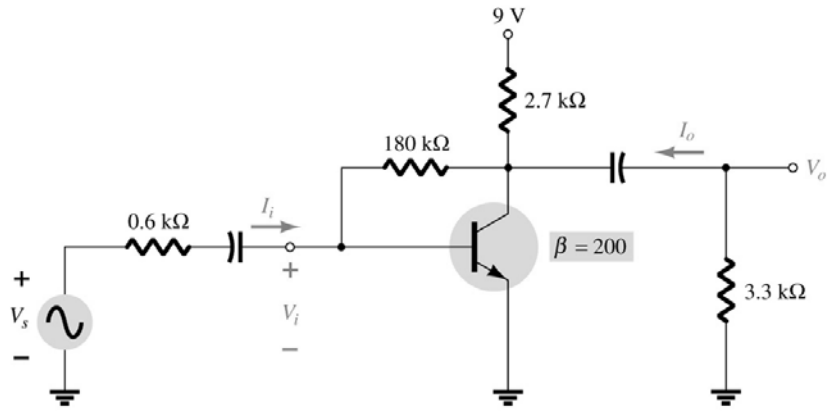
FIGURE 10-22 Collector feedback configuration with R_s and R_L .



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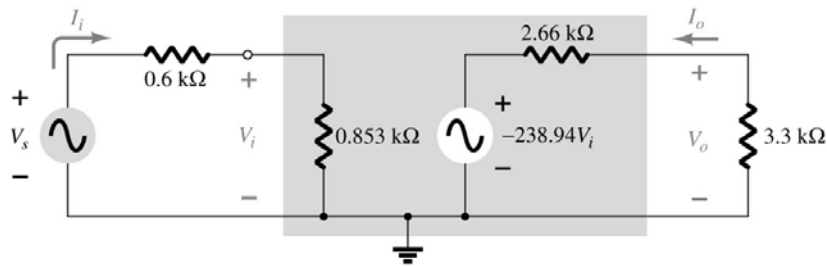
FIGURE 10-23 Example 10.5.



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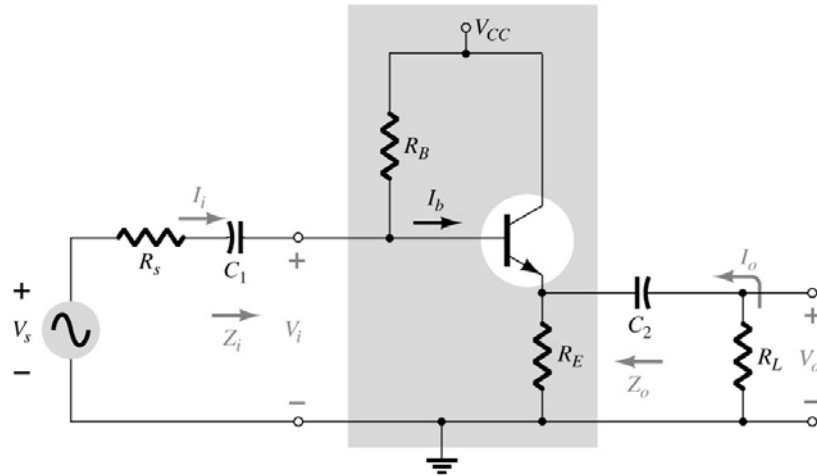
FIGURE 10-24 The ac equivalent circuit for the network of Fig. 10-23.



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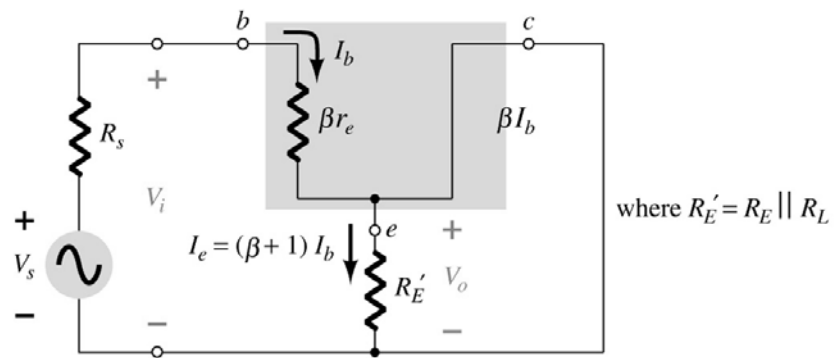
FIGURE 10-25 Emitter-follower configuration with R_s and R_L .



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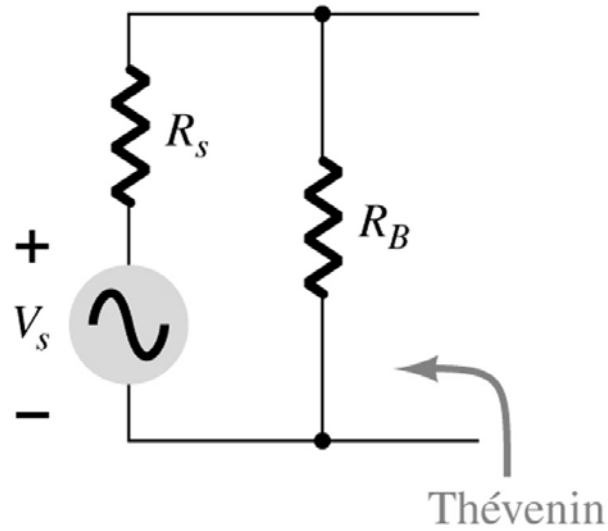
FIGURE 10-26 Emitter-follower configuration of Fig. 10-25 following the substitution of the re equivalent circuit.



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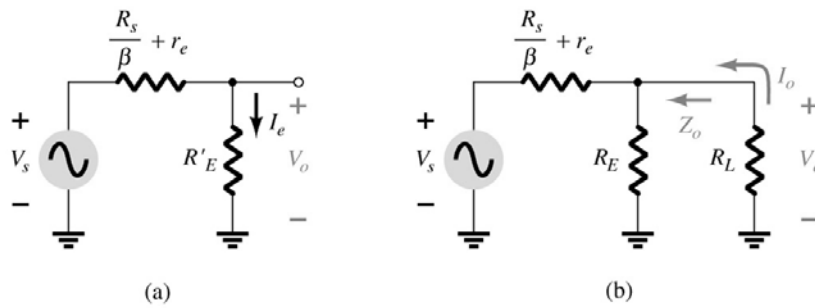
FIGURE 10-27 Determining the Thévenin equivalent circuit for the input circuit of Fig. 10-25.



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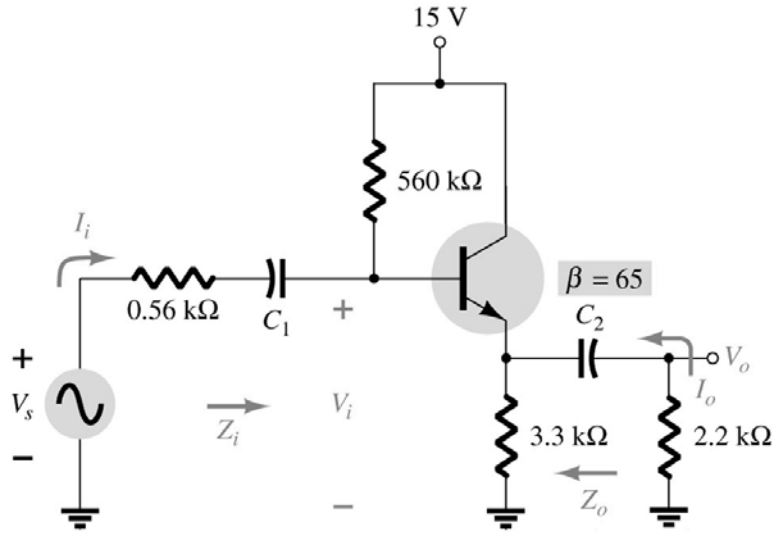
FIGURE 10-28 Networks resulting from the application of Kirchhoff's voltage law to the input circuit of Fig. 10-26.



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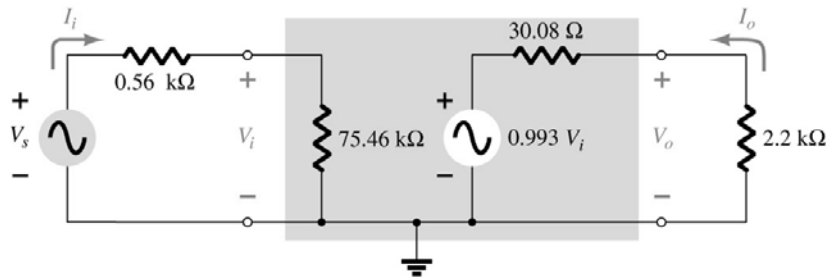
FIGURE 10-29 Example 10.6.



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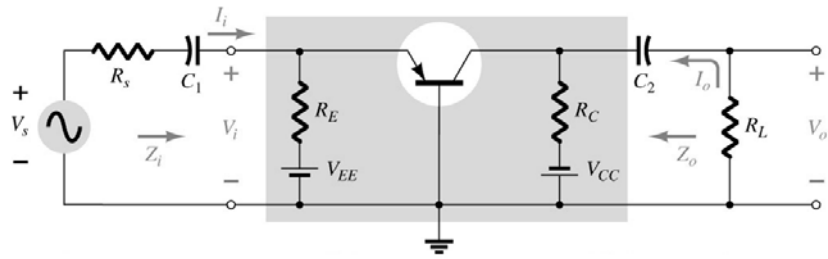
FIGURE 10-30 Small-signal ac equivalent circuit for the network of Fig. 10-29.



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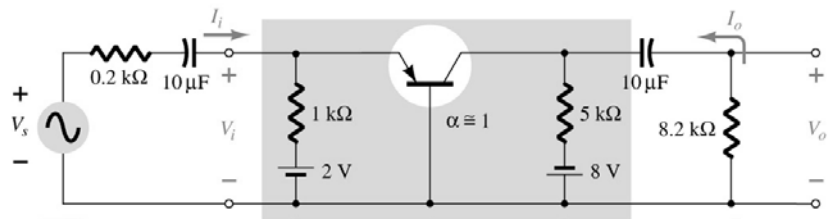
FIGURE 10-31 Common-base configuration with R_E and R_L .



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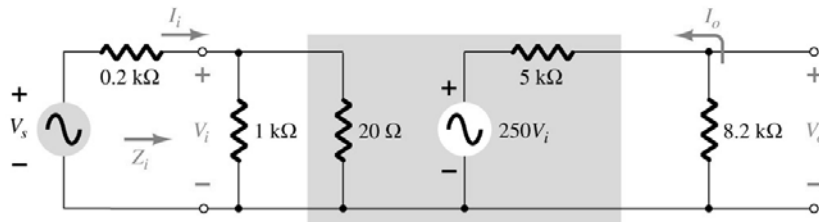
FIGURE 10-32 Example 10.7.



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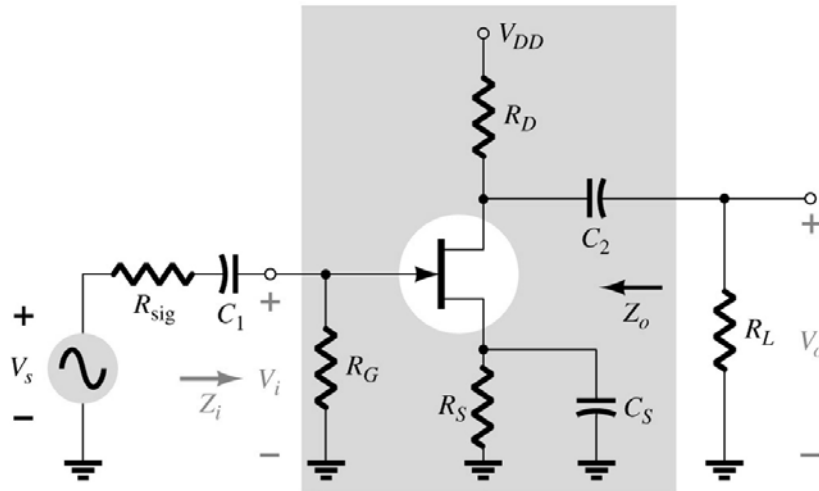
FIGURE 10-33 Small-signal ac equivalent circuit for the network of Fig. 10-32.



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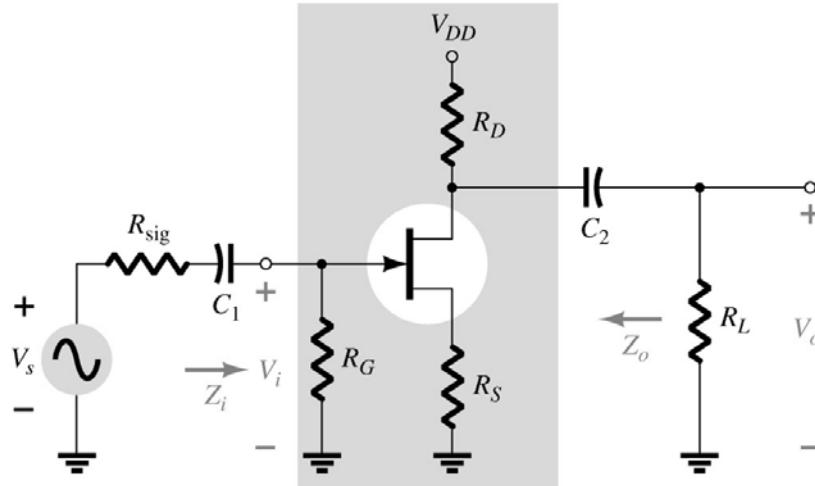
FIGURE 10-34 JFET amplifier with R_{sig} and R_L .



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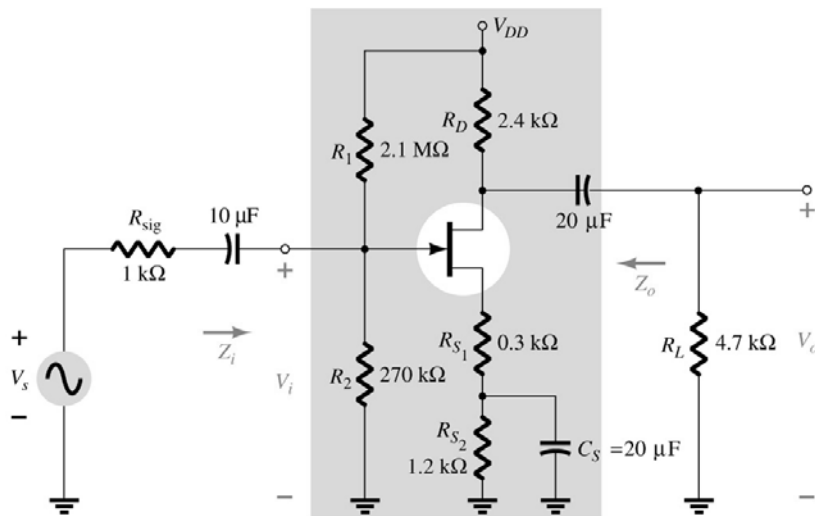
FIGURE 10-35 JFET amplifier with unbypassed R_S .



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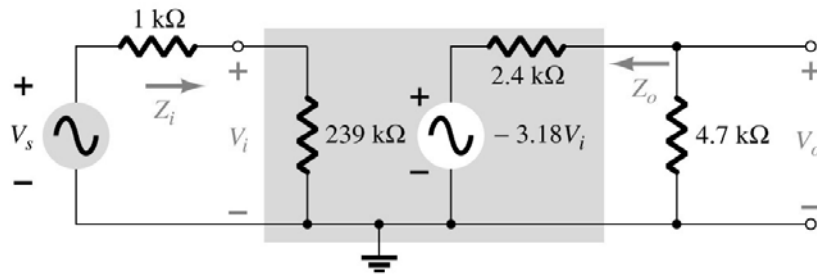
FIGURE 10-36 Example 10.8.



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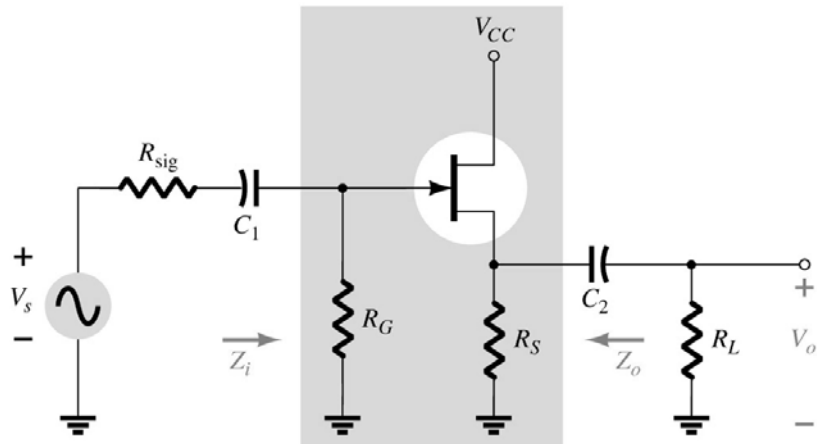
FIGURE 10-37 Small-signal ac equivalent circuit for the network of Fig. 10-36.



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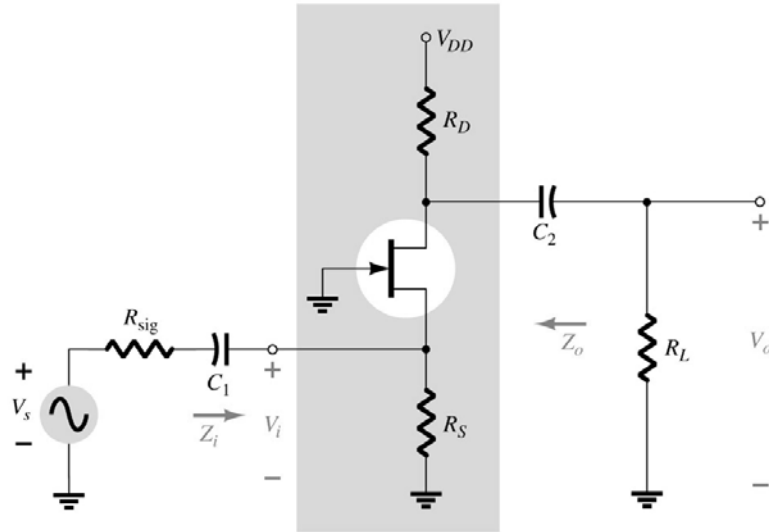
FIGURE 10-38 Source-follower configuration with R_{sig} and R_L .



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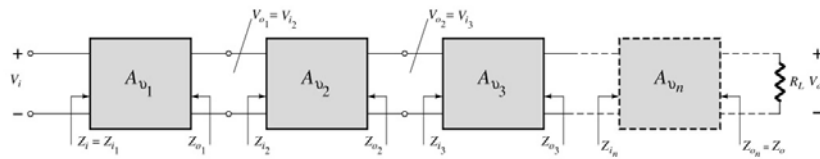
FIGURE 10-39 Commongate configuration with R_{sig} and R_L .



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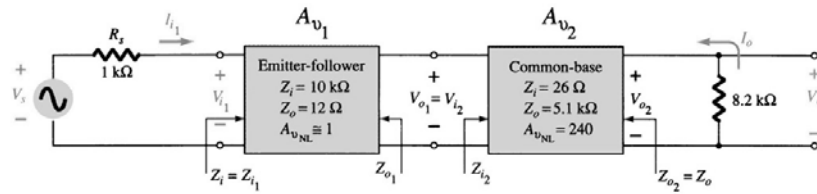
FIGURE 10-40 Cascaded system.



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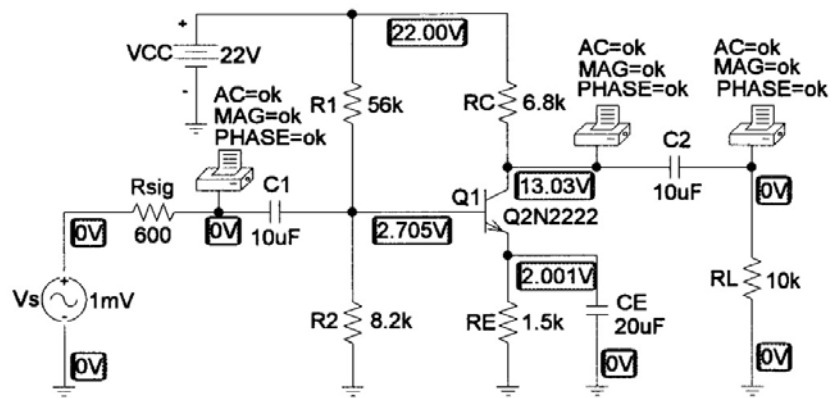
FIGURE 10-41 Example 10.9



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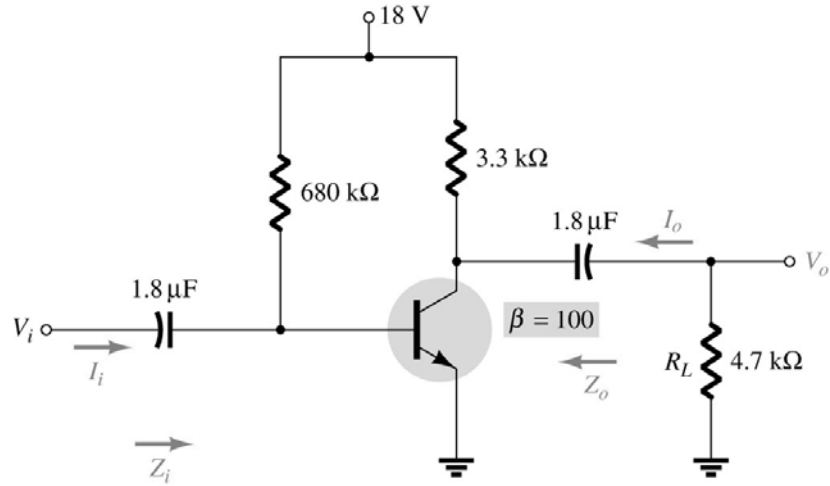
FIGURE 10-42 Loaded voltage-divider BJT transistor configuration.



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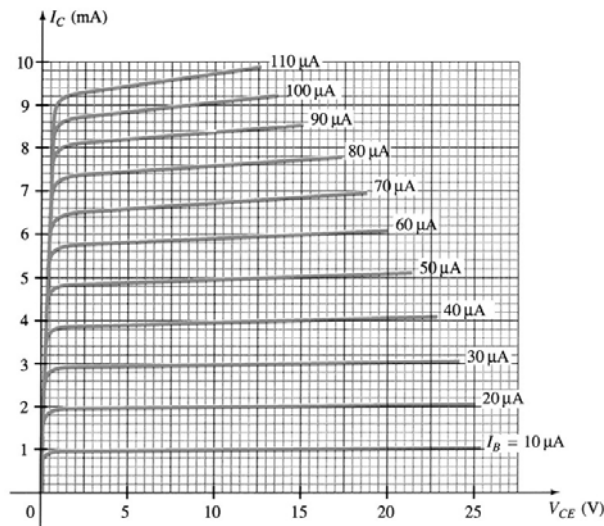
FIGURE 10-47 Problems 1, 2, and 3



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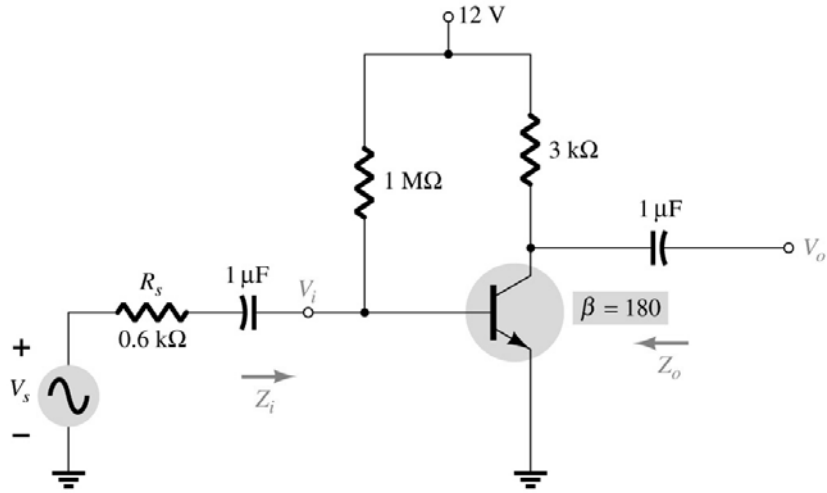
FIGURE 10-48 Problems 2 and 7



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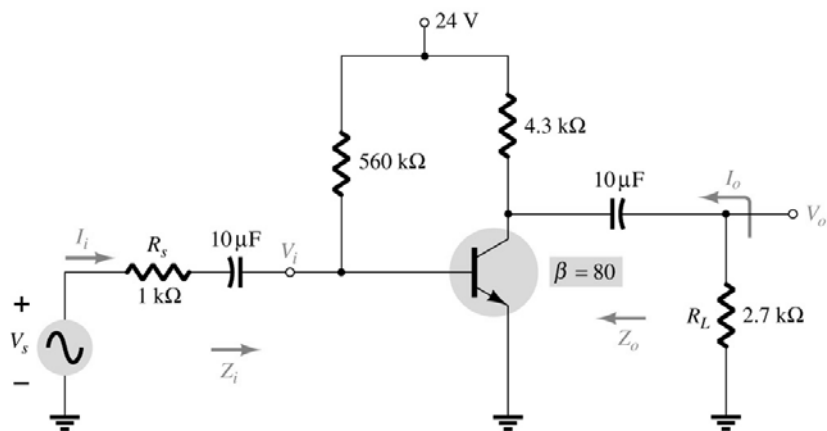
FIGURE 10-49 Problem 4



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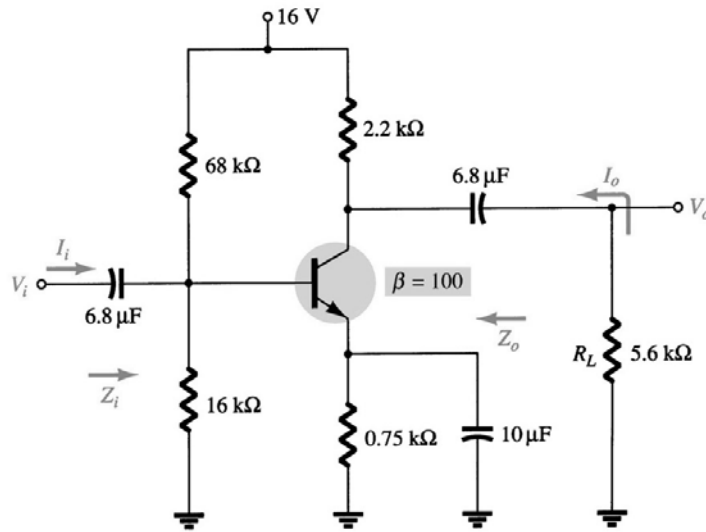
FIGURE 10-50 Problems 5, 17, and 21



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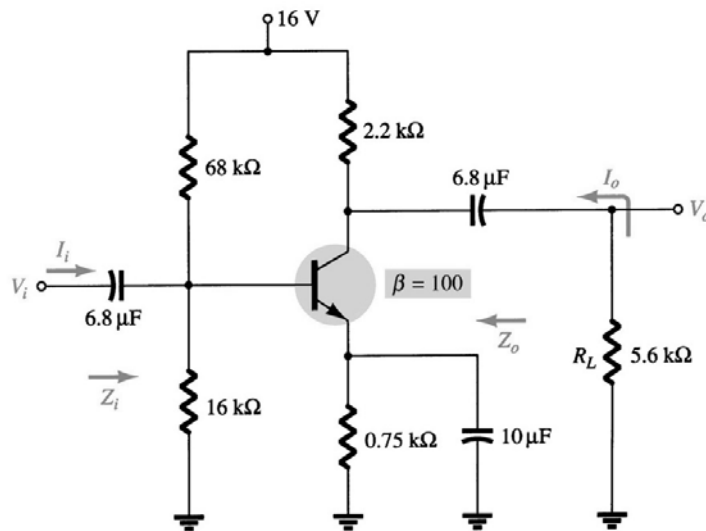
FIGURE 10-50 Problems 5, 17 and 21



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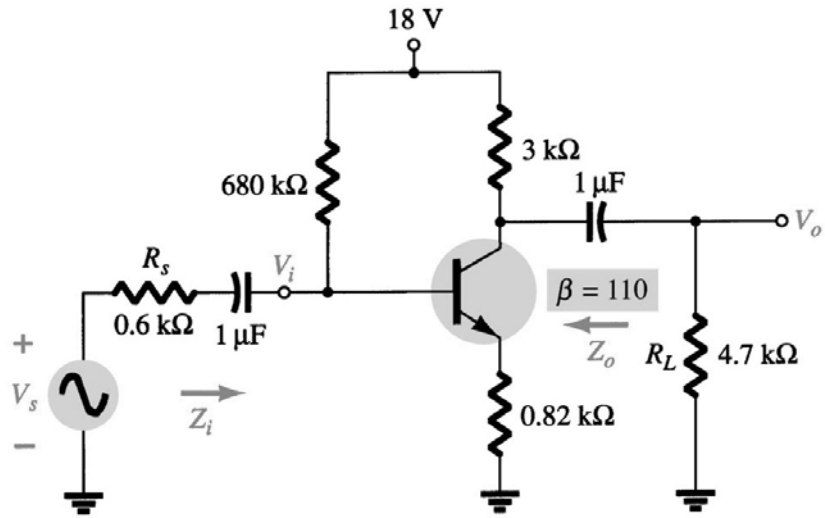
FIGURE 10-51 Problems 6, 7, and 8



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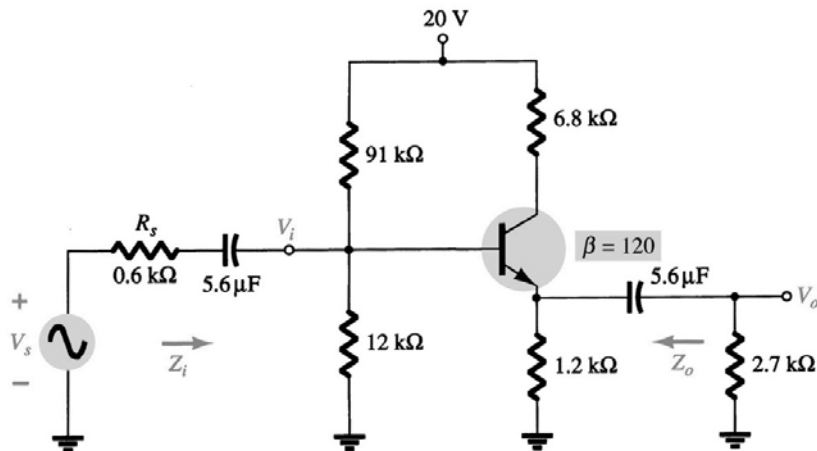
FIGURE 10-52 Problem 9



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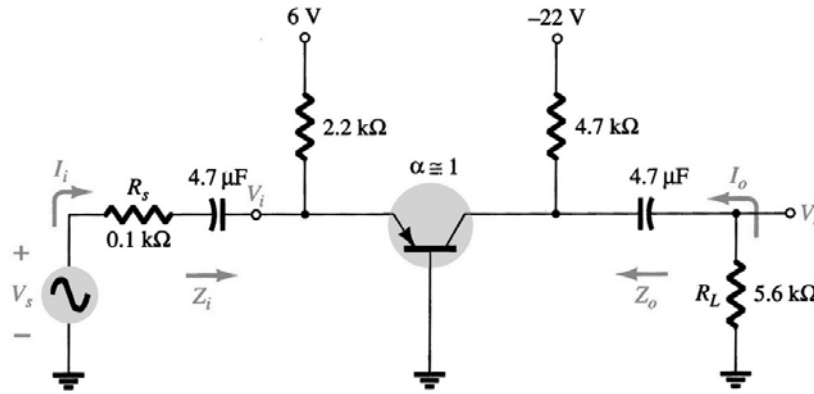
FIGURE 10-53 Problems 10 and 18



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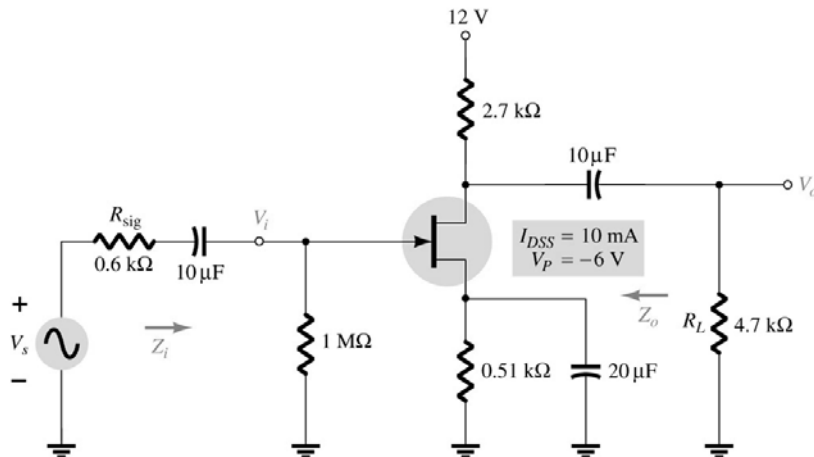
FIGURE 10-54 Problems 11, 19 and 22



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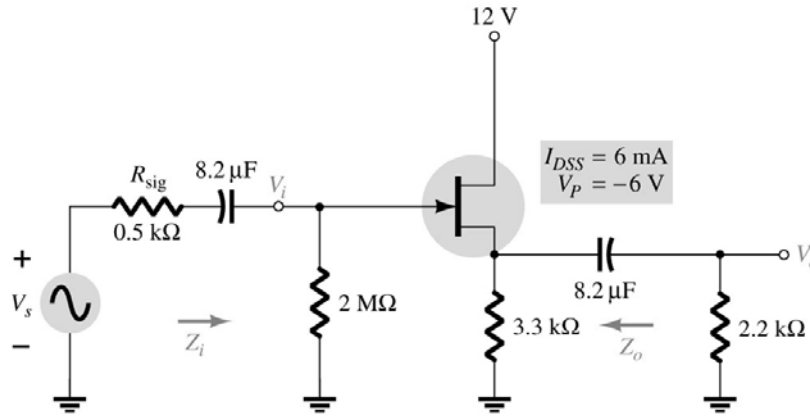
FIGURE 10-55 Problem 12 and 20



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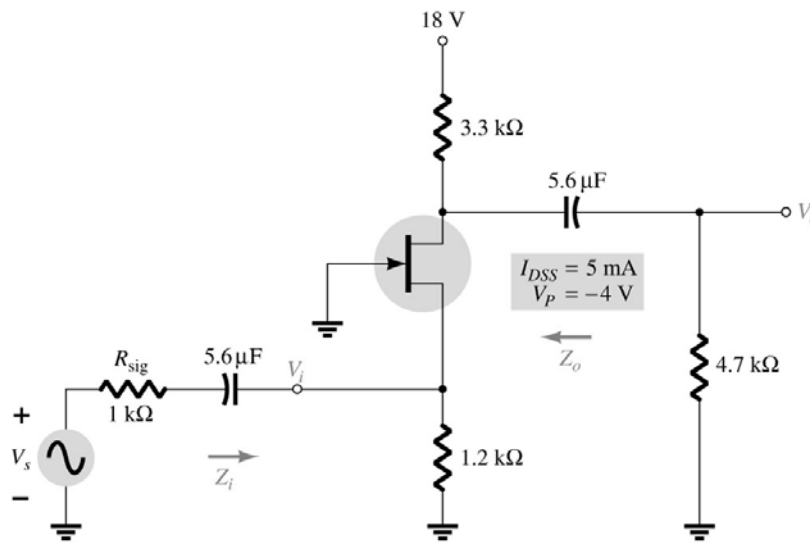
FIGURE 10-56 Problem 13



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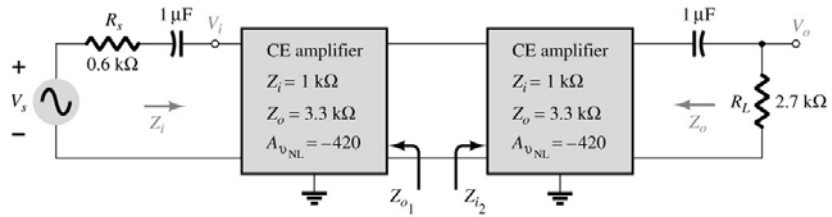
FIGURE 10-57 Problem 14



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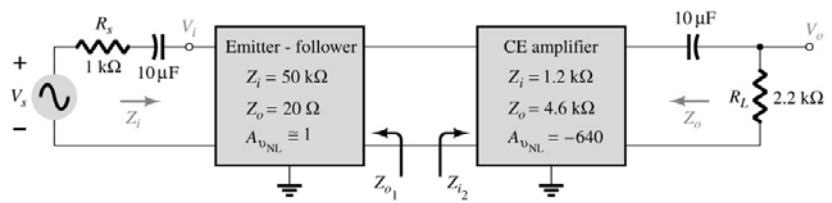
FIGURE 10-58 Problem 15



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FIGURE 10-59 Problem 16



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